

MARKED UP COPY SHOWING CHANGES

The paragraph on page 9, line 19, is modified as follows:

FIG. 9C is a [third magnified portion of the schematic diagram depicted in **FIG. 9**] chart showing the values of components in the schematic diagrams depicted in **FIGS. 9A** and **9B**.

The following paragraph was added on page 10, after the paragraph starting on line 3:

FIG. 10D is a chart showing the values of components in the schematic diagrams depicted in **FIGS. 10A-C**.

The paragraph on page 22, line 6, is modified as follows:

Turning to the input / transmitter side, a first input signal is provided to an input signal interface 204. The input signal is a wideband digital signal, either electrical or optical, according to a variety of signal types (including TCP/IP, Fast Ethernet, SONET, ATM, or other signal types known in the art, on various physical layers such as STS-3, STS-12, OC-3, or OC-12). Various electrical or fiber optic cable connectors may be received by the input signal interface 204 depending on design requirements. Upon receipt of the digital input signals, these signals are provided to a regenerator 206. The regenerator 206 preferably includes [either a limiting amplifier 207 or automatic gain control 208 to provide gain, as necessary, and smooth out variations in input signal amplitude] an input signal amplifier 207, either a limiting amplifier or an automatic gain control, to provide gain, as necessary, and smooth out variations in input signal amplitude. The regenerator

206 further includes a first clock / data recovery circuit 210 to provide protocol independence. The first clock and data recovery circuit 210 includes at least one oscillator 212, such as a crystal, to regulate the clock frequencies. When more than one oscillator is provided, the integrated circuit utilizes two phase locked loops to permit modulation as different frequencies, so as to accommodate more than one data transmission protocol, such as TCP/IP, Fast Ethernet, SONET, and ATM. Thus, a single transceiver 200 is enabled to transmit and receive more than one of the aforementioned protocols. Switching between clock frequencies may be performed by manually substituting an existing oscillator 212 with an oscillator of a different frequency. More preferably, as shown in FIG. 8, multiple oscillators 212, 213 may be built into the transceiver 200, and a switch 214 may accomplish switching between the oscillators 212, 213. This switching may be controlled manually, or, more preferably, by a controller 250, such as by using transistor-transistor logic. Either oscillator 212, 213 provides a clock signal to the data recovery electronics 215.

The paragraph on page 24, line 3, is modified as follows:

Turning to the output/receiver side, an incident laser beam is received by the laser receiving module 229 and converted to a preamplified electrical signal. The signal is provided to output signal electronics 230, which includes several elements. First the signal is provided to a second regenerator 232. The regenerator 232 preferably includes [either a limiting amplifier 234 or automatic gain control 235 to provide gain, as necessary, and smooth out variations in signal amplitude] a signal amplifier 234, either a limiting amplifier or an automatic gain control, to provide gain, as necessary, and smooth out variations in

signal amplitude. The second regenerator 232 preferably further includes a second clock / data recovery unit 236. The second clock and data recovery unit 236 preferably also comprises a switchable dual oscillator such as the dual oscillator 212, 213 shown in connection with the first clock and data recovery unit 210, and operates in a similar manner. Upon regeneration, the resulting digital electronic signal may be provided to an optional de-multiplexer 238 to segregate at least one additional output signal 205. Following de-multiplexing, the digital signal remaining in the output signal electronics 230 is passed to an output signal interface 240. An output signal interface 240 converts the electronic signal into an appropriate output signal, such as an electronic or optical signal. Either electrical or optical interfaces may be provided, subject to the inclusion of appropriate hardware as would be apparent to one skilled in the art. In one embodiment, the output signal interface 240 includes a fiber transmitter that converts the electronic signal to an optical signal, and further includes a fiber optic connector for connecting a fiber optic cable. The primary output signal is a wideband digital signal, and may be in accordance with various protocols known in the art, including TCP/IP, IPX, Fast Ethernet, SONET, or ATM, and may operate on various physical layers known in the art, including STS-3, STS-12, OC-3, or OC-12. Although depicted separately, the output signal interface 240 and input signal interface 204 may be combined, and if the interfaces 204, 240 include a fiber optic transmitter and a fiber optic receiver, then an integrated fiber optic transceiver may be used.